CLAIMS

Now, therefore, the following is claimed:

1. A computer system for processing instructions of a computer program, comprising:

a plurality of registers;

a plurality of connections corresponding respectively with said registers;

a pipeline configured to process and execute at least one of said instructions, said one instruction associated with a register identifier that identifies one of said registers;

a scoreboard coupled to said plurality of connections and to said pipeline, said scoreboard having a plurality of bits corresponding respectively with said plurality of registers, said scoreboard configured to receive said first register identifier and, in response to said first register identifier, to assert one of said bits that corresponds with said one register, said scoreboard configured to receive a second register identifier identifying at least said one register and, in response to said second register identifier, to deassert said one bit, said scoreboard further configured to transmit said one bit across one of said connections, said one bit indicative of whether a pending write to said one register exists based on a value of said one bit and based on which of said connections is transmitting said one bit; and

hazard detection circuitry coupled to said plurality of connections, said hazard detection circuitry configured to receive said one bit and to detect whether a data hazard exists based on said one bit.

2. The system of claim 1, wherein said scoreboard is further configured to transmit a data word including each of said plurality of bits to said hazard detection circuitry, each asserted bit in said data word indicating that a different one of said registers is associated with a pending write.

3. The system of claim 1, wherein said scoreboard includes a plurality of registers, each of said registers containing a different one of said bits and connected to a different one of said connections.

4. The system of claim 1, wherein said first register identifier is a decoded register identifier, said system further comprising:

a decoder configured to receive an encoded register identifier defined by said instruction and to decode said encoded register identifier into said decoded register identifier, said decoder further configured to transmit said decoded register identifier to said scoreboard.

5. The system of claim 4, wherein said decoder is further configured to transmit said decoded register identifier to said hazard detection circuitry.

6. The system of claim 4, wherein said decoded register identifier includes a plurality of bits, wherein one of said bits in said decoded register identifier that corresponds to said one register is asserted, and wherein the remaining bits in said decoded register identifier are deasserted.

7. A system for processing instructions of computer programs, comprising:

a plurality of registers;

a plurality of connections, each of said connections corresponding to a different one of said registers;

means for maintaining a plurality of bits and for indicating via said bits which of said registers is associated with a pending write, said maintaining means configured to transmit said bits across said connections, wherein each bit transmitted across each of said connections is indicative of whether the register corresponding to said each connection is associated with a pending write; and

hazard detection circuitry configured to detect data hazards based on said bits transmitted across said connections.

8. The system of claim 7, wherein said maintaining means includes a plurality of registers, each of said registers containing a different one of said bits and connected to a different one of said connections.

9. The system of claim 7, further comprising:

means for processing an instruction; and

means for decoding an encoded register identifier associated with said instruction into a decoded register identifier, said decoding means configured to transmit said decoded register identifier to said hazard detection circuitry and to said maintaining means, said decoded register identifier identifying one of said registers,

wherein said hazard detection circuitry is configured to detect a data hazard based on said decoded register identifier and said maintaining means is configured to modify one of said bits based on said decoded register identifier, said one bit corresponding to said one register.

10. The system of claim 9, wherein said decoded register identifier includes a plurality of bits, wherein one of said bits in said decoded register identifier that corresponds to said one register is asserted, and wherein the remaining of said bits in said decoded register identifier are deasserted.

11. A method for processing instructions of computer programs, comprising the steps of:

providing a plurality of registers;

maintaining a plurality of bits, each of said bits indicating whether a corresponding one of said registers is associated with a pending write;

transmitting a data word, said data word including each of said bits, wherein each asserted bit in said data word indicates that a different one of said registers is associated with a pending write;

receiving said data word; and

detecting a data hazard based on said data word.

12. The method of claim 11, further comprising the steps of:

processing an instruction;

receiving an encoded register identifier associated with said instruction;

decoding said encoded register identifier into a decoded register identifier;

comparing said decoded register identifier to another register identifier;

detecting a data hazard based on said comparing step; and

modifying one of said bits based on said decoded register identifier.

13. A method for processing instructions of computer programs, comprising the steps of:

providing a plurality of registers;

maintaining a plurality of bits, each of said bits respectively corresponding with one of said registers;

providing a plurality of connections, each of said connections respectively corresponding with one of said registers;

indicating, via said bits, which of said registers are associated with pending writes;

transmitting one of said bits corresponding with a particular one of said registers across a particular one of said connections, said particular one connection corresponding with said particular one register; and

detecting a data hazard based on said one bit transmitted across said particular one connection.

14. The method of claim 13, further comprising the steps of:

processing an instruction;

receiving a register identifier associated with said instruction;

comparing a bit of said register identifier with said particular one bit transmitted across said particular one connection; and

performing said detecting step based on said comparing step.

15. The method of claim 13, further comprising the steps of:

processing an instruction;

receiving an encoded register identifier associated with said instruction;

decoding said encoded register identifier into a decoded register identifier;

comparing said decoded register identifier to another register identifier;

detecting a data hazard based on said comparing step; and

asserting one of said bits based on said decoded register identifier.